

WHAT IS CLAIMED IS:

1. A method of forming a gate in a non-volatile memory device comprising:
5 forming a tunnel dielectric layer on a semiconductor substrate;
forming a floating gate layer on the tunnel dielectric layer;
forming an intergate dielectric layer on the floating gate layer;
forming a control gate layer comprising an in-situ doped silicon layer on the intergate
dielectric layer;
10 annealing the control gate layer; and
patterning the control gate layer, the intergate dielectric layer and the floating gate
layer.

2. The method as claimed in claim 1, wherein forming a floating gate layer
15 comprises forming polysilicon.

3. The method as claimed in claim 2, wherein forming a floating gate layer
comprises forming amorphous silicon.

20 4. The method as claimed in claim 1, wherein the intergate dielectric layer
comprises an oxide/nitride/oxide (ONO) film.

5. The method as claimed in claim 1, wherein the control gate layer comprises
polysilicon.

25 6. The method as claimed in claim 1, wherein the control gate layer comprises
amorphous silicon.

7. The method as claimed in claim 1, wherein annealing the control gate layer
30 comprises furnace annealing.

8. The method as claimed in claim 7, wherein the furnace annealing is performed
at a temperature of about 600~950°C.

9. The method as claimed in claim 1, wherein annealing the control gate layer comprises rapid thermal annealing (RTA).

10. The method as claimed in claim 9, wherein the RTA is performed at a
5 temperature of about 800~1,000°C.

11. A method of forming a gate in a non-volatile memory device, the method comprising:

10 forming a tunnel dielectric layer on a semiconductor substrate;
forming a first silicon layer as a floating gate layer on the tunnel dielectric layer;
forming an oxide-nitride-oxide (ONO) intergate dielectric layer on the first silicon
layer;
forming a second silicon layer as a control gate layer on the ONO layer;
forming a metal silicide layer on the second silicon layer;
15 annealing the resultant structure; and
 patterning the metal silicide layer, the second silicon layer, the ONO layer and the first
silicon layer.

12. The method as claimed in claim 11, wherein forming a first silicon layer
20 comprises forming polysilicon.

13. The method as claimed in claim 11, wherein forming a first silicon layer
comprises forming amorphous silicon.

25 14. The method as claimed in claim 11, wherein forming a second silicon layer
comprises forming polysilicon.

15. The method as claimed in claim 11, wherein forming a second silicon layer
comprises forming amorphous silicon.

30 16. The method as claimed in claim 11, wherein performing an annealing process
comprises furnace annealing.

17. The method as claimed in claim 16, wherein the furnace annealing is performed at a temperature of about 600~950°C.

18. The method as claimed in claim 11, wherein performing an annealing process
5 comprises rapid thermal annealing (RTA).

19. The method as claimed in claim 18, wherein the RTA is performed at a temperature of about 800~1,000°C.

10 21. A method of forming a gate in a non-volatile memory device, the method comprising:

forming a tunnel dielectric layer on a semiconductor substrate;

forming a first silicon layer on the tunnel dielectric layer;

forming an oxide-nitride-oxide (ONO) intergate dielectric layer on the first silicon

15 layer;

forming a second silicon layer as a control gate layer on the ONO layer;

forming a metal silicide layer on the second silicon layer;

annealing the resultant structure to reduce a thickness variation of the ONO layer and to reduce a bird's beak phenomenon at the interface between the ONO layer and the second
20 silicon layer; and

sequentially patterning the metal silicide layer, the second silicon layer, the ONO layer and the first silicon layer.

22. The method of claim 21, wherein the annealing is performed in an ambient
25 including an inert gas.

23. The method of claim 21, wherein forming a metal silicide layer comprises using dichlorosilane gas to form a tungsten silicide layer.

30 24. The method of claim 23, wherein the annealing is performed after forming the tungsten silicide layer.